5 Gb/s Burst-Mode Clock Phase Aligner with (64, 57) Hamming Codes for GPON Applications

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Abstract

digital PLL, is limited to an operating range of 24 MHz to 500 MHz. The latter frequency is 20 times slower than the targeted 10 Gb/s (2 oversampling of the 5 Gb/s data). Thus, two stages of deserialization are employed.

The first deserialization stage is performed by the off-board 1:16 deserializer. The oversampled 10 Gb/s data and clock are deserialized to 34 parallel signals (32 differential data signals + 2 differential clock signals), each at 625 Mb/s each. These signals are then brought on to the FPGA board through low-voltage differential signaling. However, the 625 MHz clock signal is 1.25 faster than the maximum operating frequency of DCM which is 500 MHz. Thus, a clock divider is used to reduce the frequency of the received clock to 312.5 MHz. This clock signal is then fed to a DCM block for further clock distribution throughout the system.

The second deserialization stage is based on the DDR signaling, and it is accomplished by a 1:8 deserializer designed and implemented on the FPGA. It uses the 312.5 MHz DCM output clock signal to sample the 625 Mb/s incoming data at both the rising and the falling clock edges DDR signaling. In this way, each data signal is separated into two data lines by a half-rate clock signal. The same clock is then used to demultiplex these two lines of data into an 8-bit data path. In summary, the 16 input data signals are deserialized to 128 data lines at 78 Mb/s which is eight times lower than 625 Mb/s. The advantage of this method is that the clock signal is well within the 24 MHz to 500 MHz operating range of the DCM guaranteeing system synchronization while keeping the same harmonic content of the clock and data lines.

C. Clock and Phase Alignment

The idea behind the CPA is based on a simple, fast, and effective algorithm. Since the data is sampled twice per bit, the odd samples and even samples (O and E, respectively, in Fig. 2), sampled on the alternate (odd and even) clock rising edges are identical. The odd samples are forwarded to path O and the even samples are forwarded to path E. The byte synchronizer is responsible for detecting the delimiter. It makes use of a payload detection algorithm to look for a preprogrammed delimiter. The two byte synchronizer attempt to detect the delimiter on either the odd and/or even samples of the data respectively. That is, regardless of the phase step between two consecutive packets (2π rads), there will be at least one clock edge (odd or even) that will yield an accurate sample. The phase picker then uses feedback from the byte synchronizers to select the right path from the two possibilities. The realigned data is then sent to the BERT.

In essence, the BM-CPA supports three modes of operation: $1)$ conventional mode essentially a SONET CDR, $2)$ burst-mode with CDR CPA turned ON with CDR locking at twice the data rate, $3)$ burst-mode with LO CPA turned ON with LO locking at twice the data rate. These modes of operation are useful in measuring the relative performances.

D. Hamming Decoder

A Hamming code is a linear error-correcting code, in which parity symbols are appended to original data for error detection and correction [2]. More specifically, a (p, k) Hamming codeword has a length of p bits, out of which k bits are information bits, and $p \quad k$ are check bits, also known as parity bits. Conventional Hamming code has minimum distance of 3, which allows either single error correction or double error detection, but not both. Optimal minimum odd-weight-column single error correction double error detection (SEC-DED) code is a shortened version of Hamming code. It has better performance, cost, and reliability than conventional Hamming code [3]. The shortened Hamming code's parity-check matrix is constructed by deleting certain columns from the conventional Hamming parity-check matrix to insure a minimum distance of 4. Thus, SEC-DED can be performed at the same time. The reconstruction of the the parity-check matrix also reduces the complexity of the decoder design and features more cost-effective hardware implementation.

We implement (64, 57) shortened Hamming codes in the receiver design. In which case, every 57 bits of data is concatenated with 7 bits of parity to make a codeword of 64 bits in length. The check bits are encoded from XORing

III. Results and Discussion

Fig. 4 shows the experimental setup to measure the phase acquisition time of the BM-CPA in the three modes of operation. Bursty upstream PON traffic is generated by adjusting the phase 2π $\Delta\varphi$ $+2\pi$ rads on a 1-ps resolution, between alternating packets from two programmable ports of a pattern generator, which are then concatenated via a radio frequency power combiner (PC). These packets are formed from: preamble bits, 36 delimiter bits, 2^{15} 1 payload bits, and 48 comma bits. The preamble field is used to perform amplitude and phase recovery. We define the phase acquisition time as the number of preamble bits needed to achieve error-free operation (PLR $< 10^{-6}$ and BER $< 10^{-10}$) for any phase step $j\Delta\varphi j$ 2π rads, between consecutive packets. The delimiter is a unique pattern indicating the start of the packet to perform byte synchronization. Likewise, the comma is a unique pattern to indicate the end of the payload. The payload is simply a nonreturn-to-zero 2^{15} 1 PRBS. The PLR and the BER are measured on the payload bits only.

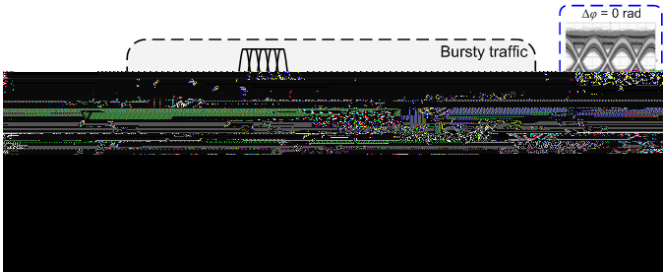

Fig. 4. Experimental setup (LPF: low-pass filter).

A. PLR Measurements

Fig. 5 shows the PLR performance of the system as a function of the phase difference between consecutive packets. Fig. 5(a) depicts the phase step response of the receiver with

system may be severely impaired by the mode-partition noise (MPN) of the FP laser coupled with the chromatic dispersion that exists in the transmission fiber [5].

To study the impact of FEC on the optical budget of the GPON uplink, we plot the BER performance of the system with and without FEC, as a function of the received power as shown in Fig. 6. According to the G.984.2 standard, coding gain is defined as the difference in input power at the receiver with and without FEC at a BER $= 10^{-10}$. With the implemented (64, 57) Hamming codes, we observe a coding gain of 1.8 dB.

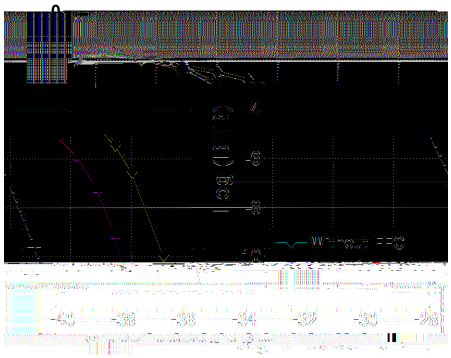

Fig. 6. BER performance for the BM-CPA.

It is interesting to compare the performance of the (64, 57) Hamming codes, a class of binary linear codes, with the well-known (255, 239) Reed-Solomon (RS), a nonbinary subclass of multiple-error-correcting BCH codes [2]. The block-based RS codes defined as $RS(n, k)$, divide a codeword into n symbols of m bits each, of which k are data (uncoded) symbols. In a memoryless channel, a symbol-error rate after FEC p^{FEC}