Experimental Demonstration of a SAC-OCDMA PON With Burst-Mode Reception: Local Versus Centralized Sources

Fig. 1. SAC-OCDMA PON physical architecture: (a) LS architecture; (b) CLS architecture.

RN consists of passive combiners and splitters, as in existing

Fig. 2. (a) Typical burst-mode uplink test signal used to test the phase acquisition time of the clock phase aligner. (b) Block diagram of the OLT burst-mode receiver for SAC-OCDMA PONs (DES: deserializer; Sync: synchronizer).

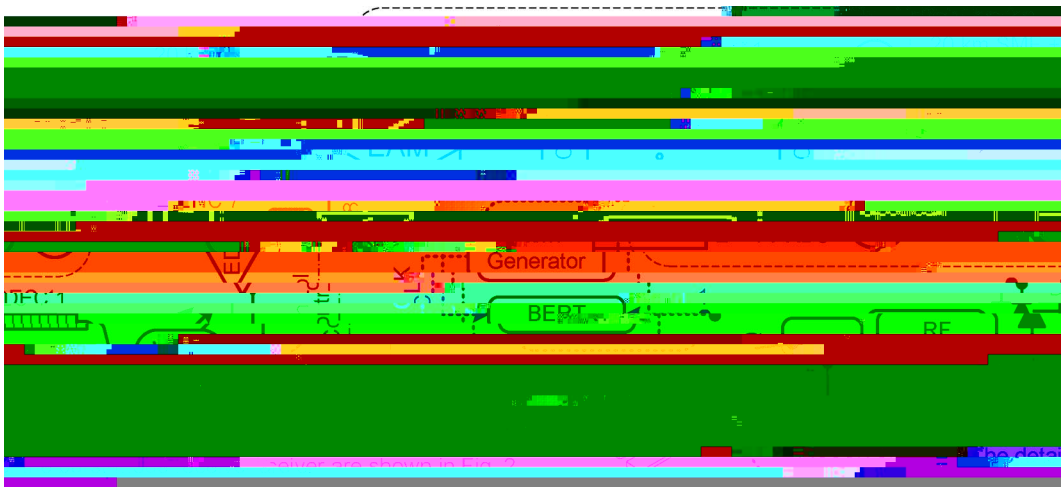

Fig. 3. Experimental setup for a 7 × 622 Mb/s SAC-OCDMA PON uplink (BERT: BER tester; CLK: clock; DEC: decoder; and ENC: encoder).

pattern to indicate the end of the payload. The payload is simply a $2^{15} - 1$ pseudorandom binary sequence (PRBS). The BER and PLR are measured for the payload bits only. The lock acquisition time corresponds to the number of bits (n) in front of the delimiter in order to get a zero PLR for over 3 min at 622 Mb/s ($> 10^6$ packets received, i.e., PLR $< 10^{-6}$), a BER $< 10^{-10}$, and for any phase step $(-2\pi \leq \Delta\varphi \leq +2\pi)$ between consecutive packets [19]. We will demonstrate that even at $n = 0$, i.e., no preamble bits, our phase picker gives excellent results. To generate alternating packets with adjustable phase, as in Fig. 2(a), we combined two programmable ports from the HP80000 pattern generator shown in Fig. 3 using a radio frequency (RF) power combiner. The phase steps between the consecutive packets can be set anywhere between ± 2 ns on a 2-ps resolution, corresponding to a ± 1.25 unit interval (UI) at 622 Mb/s. Note that 1 UI corresponds to 1-bit period.

A. Building Block Diagrams

The main building blocks of the SAC-OCDMA burst-mode receiver we designed are illustrated in Fig. 2(b). The receiver includes a multirate SONET CDR from Analog Devices (Part #ADN2819), a $1:8$ deserializer from Maxim-IC (Part #MAX3885), and a CPA module and a FEC RS(255,239) decoder implemented on a Virtex II Pro FPGA from Xilinx. Our receiver without the CPA is therefore similar to that in [20], but without the return-to-zero (RZ) to nonreturn-to-zero (NRZ) converter needed for FFH-OCDMA. The receiver also avoids the use of an $8:1$ serializer (used with FFH-OCDMA) to up convert the frequency. The quantizer (Q) is used before the CDR to threshold the incoming signal to filter out intensity noise and other channel impairments. The threshold is manually adjusted to sample in the middle of the eye opening to obtain the optimum BER. The multirate CDR then recovers the clock and data from the incoming signal. The receiver is operated at either 622 or 666.43 Mb/s depending on whether the FEC module is OFF or ON, respectively. The CDR is followed by a $1:8$ deserializer (DES) that reduces the frequency of the recovered clock and data to a frequency that can be processed by the digital logic. Afterwards, a framer, a comma detector, a CPA (including a phase picker and byte synchronizers), phase locked loops (PLLs), an RS(255,239) decoder, and a custom BERT are implemented on an FPGA. Note that a computer is used to control the output of the pattern generator and to communicate with the FPGA on the receiver (Fig. 3). Automatic detection of the payload is implemented on the FPGA through a comma detector and a framer, which are responsible for detecting the beginning (delimiter bits) and the end (comma bits) of the packets, respectively, as in [20]. The CPA module makes use of the phase picking algorithm in [19] and the CDR operating at $2\times$ oversampling. The CPA is turned ON for the PLR measurements with phase acquisition; otherwise, it is bypassed. The CPA is then followed by the RS decoder and the FPGA-based BERT.

B. Burst-Mode Receiver Functionalities

The idea behind the CPA is based on the simple, fast, and effective algorithm in [19]. Since the CDR samples the data twice per bit, the odd samples and even samples [O and E, respectively, in Fig. 2(b)], sampled on the alternate (odd and even) clock rising edges (t_{odd} and t_{even} in Fig. 12) are identical. The odd samples are forwarded to path O and the even samples to path E. The byte synchronizer is responsible for detecting the delimiter. It makes use of a payload detection algorithm to look for a preprogrammed delimiter. The idea behind the phase picking algorithm is to replicate the byte synchronizer twice in an attempt to detect the delimiter on either the odd and/or even samples of the data, respectively. That is, regardless of any phase step, i.e., $-2\pi \leq \Delta\varphi \leq +2\pi$, between consecutive packets, there will be at least one clock edge (either t_{odd} or t_{even}) that will yield an accurate sample. The phase picker then uses feedback from the byte synchronizers to select the correct path from the two possibilities. For further illustration, we refer the reader to Fig. 12, where the CDR output for the $2\times$ over sampling mode at specific three possible phase differences between consecutive packets is shown.

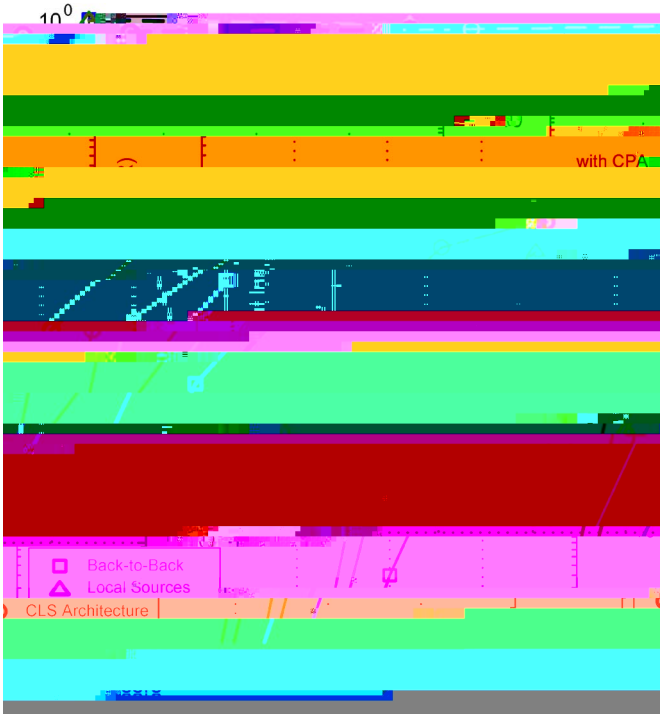

Fig. 10. PLR versus number of users for different PON architectures (dashed lines for the system without CPA; solid lines for the system with CPA).

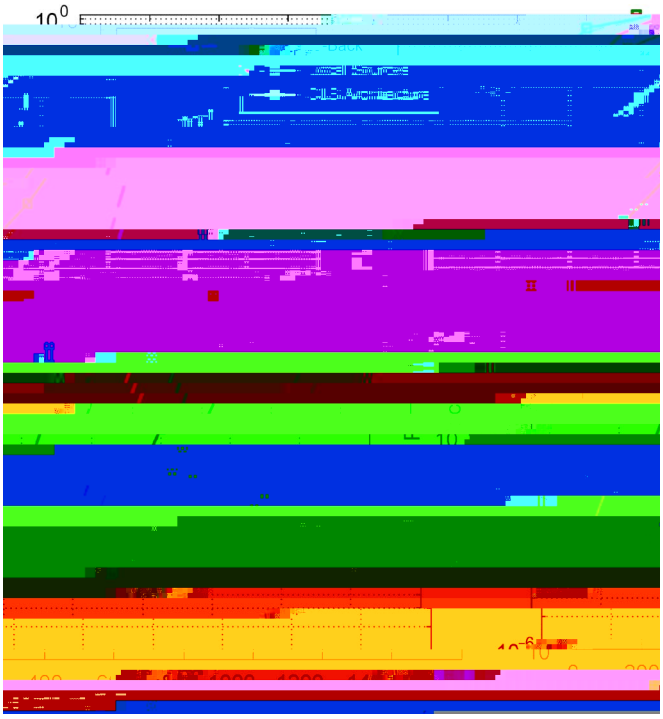

Fig. 11. PLR versus length of CID for different PON architectures.

are for lost up to four users for the three different architectures (PLR $< 10^{-6}$). Increasing the number of users beyond four deteriorates the BER and thus the PLR. For a fully loaded PON

Fig. 12. Response of the CDR to bursty traffic (packets with different phases): (a) no phase difference; (b) $\pi/2$ phase difference; (c) π phase difference.

additional fiber attenuation in CLS architectures, respectively. In CLS architectures, an EDFA can be used at the central office to increase the margin by compensating the extra losses terms in (3). Using a semiconductor optical amplifier (SOA) or a reflective SOA at ONU for modulation instead of the EAM reduces the amplification requirements

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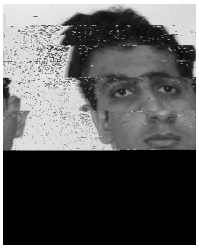

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